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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/693,568	10/24/2003	Patrick Lysaght	X-1374 US	1995

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EXAMINER	
LEVIN, NAUM B	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 08/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/693,568	LYSAGHT ET AL.	
	Examiner	Art Unit	
	Naum B. Levin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/24/03, 10/22/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-2, 4, 6-8 and 11-20 are rejected under 35 U.S.C. 102(b) as being unpatentable by Dean et al. (US Patent 6,269,468).

2. As to claims 1, 11, 14 and 17 Dean discloses:

(1), (11), (14) A method/program/machine of designing an integrated circuit having a plurality of logic paths, comprising (col.6, ll.22-23, col.7, ll.37-41):

designing the integrated circuit in accordance with timing constraint (requirement) data (col.5, ll.12-28);

identifying any logic paths (circuit paths/paths) in said plurality of logic paths that have a timing characteristic within a threshold to define a first set of logic paths (non-critical paths), where any logic paths in said plurality of logic paths other than said first set of logic paths define a second set of logic paths (critical paths) (col.5, ll.28-52; col.7, ll.42-44); and

selectively optimizing the integrated circuit to reduce power consumption in response to said first set of logic paths and said second set of logic paths (col.5, ll.52-59; col.8, ll.10-14);

(17) A method of designing an integrated circuit, comprising:

designing the integrated circuit in accordance with timing constraint data (col.5, ll.12-28);

identifying timing critical logic circuitry (col.5, ll.28-52; col.7, ll.42-44); and

selectively optimizing the integrated circuit to reduce power consumption in response to said timing critical circuitry (col.5, ll.52-59; col.8, ll.10-14).

3. As to claims 2, 4, 6-8, 12-13, 15-16 and 18-20 Dean recites:

(2), (12), (15) The method/program/machine, wherein said selectively optimizing comprises power optimizing only said second set of logic paths (col.5, ll.52-54);

(4), (7), (13), (16), (18), (19), (20) The method/program/machine, wherein said selectively optimizing comprises power optimizing said first set of logic paths and said second set of logic paths, and determining whether said timing characteristic of any logic paths in said first set of logic paths has been modified beyond a threshold to define a third set of logic paths (col.5, ll.57-59; col.5, ll.66-67; col.6, ll.1-7);

(6), (8) The method comprises rejecting a power optimization for each logic path in the third set of logic paths (col.5, ll.52-59; col.5, ll.66-67; col.6, ll.1-7; col.8, ll.10-14).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3, 5, 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dean in view of Patra et al. (US Patent 6,721,924).

With respect to claims 3, 5, 9 and 10 Dean teaches the features above but lacks a method of designing an integrated circuit having a plurality of logic paths, wherein power optimizing comprises placing first and second set of logic with respect to target device, and routing connections of said first an second set of logic paths.

As to claims 3, 5, 9 and 10 Patra teaches:

(3), (5) A method of designing an integrated circuit having a plurality of logic paths, wherein power optimizing comprises placing first and second set of logic with respect to target device, and routing connections of said first an second set of logic paths (col.3, ll.23-55; col.6, ll.24-43);

(9), (10) The method, wherein said threshold is defined by an value (maximum/minimum delay) with respect to a parameter (delay) of said timing constraint data (col.5, ll.8-58).

It would have been obvious to a person of ordinary skills in the art at the time the invention was made to employ Patra's teaching regarding the method of designing an integrated circuit having a plurality of logic paths, wherein power optimizing comprises placing first and second set of logic with respect to target device, and routing connections of said first an second set of logic paths to increase completeness of the integrated circuit design.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B. Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Naum Levin

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Naum Levin

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